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5. The device of claim 1 wherein said portion of said extended trench is narrower than said upper portion.

6. The device of claim 1 wherein said upper layer is an epitaxial layer.

7. The device of claim 1 wherein said substrate comprises monocrystalline silicon.

8. The device of claim 1 wherein said dielectric material comprises silicon dioxide.

9. The device of claim 1 wherein said conductive material in said trench comprises doped polysilicon.

10. The device of claim 1 wherein said first conduction type is N and said second conduction type is P.

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11. The device of claim 1 wherein said device comprises a plurality of extended trenches.

12. The device of claim 11 wherein said plurality of extended trenches have an open-cell stripe topology.

13. The device of claim 11 wherein said plurality of extended trenches have a closed-cell cellular topology.

14. The device of claim 1 selected from the group consisting of a power MOSFET, an insulated gate bipolar transistor, and an MOS-controlled thyristor.

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